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[Title of the Invention]

Method of Manufacturing A Semiconductor Device

[Abstract]

[Object] The present invention provides a method of manufacturing a thin film transistor using a polycrystalline silicon film as an active layer. The method eliminates variation in the characteristics which accompanies an enlarged grain size of the polycrystalline silicon film.

[Constitution] In order to attain the aforementioned purpose, according to the present invention, first, before solid phase crystallization of an amorphous silicon film, a region where a crystal nucleus is formed with priority is selectively formed in the film.

[Scope of Claims]

[Claim 1] A method of manufacturing a semiconductor device for forming a polycrystalline semiconductor film by solid phase crystallization of an amorphous semiconductor film, the method being characterized in that:

a region where a crystal nucleus is generated with priority is selectively formed in said amorphous semiconductor film before said solid phase crystallization.

[Claim 2] A method of manufacturing a semiconductor device as claimed in claim 1, characterized in that said region where a crystal nucleus is formed with priority is formed by selectively forming a heavily doped impurity region.

[Claim 3] A method of manufacturing a semiconductor device as claimed in claim 1, characterized in that said region where a crystal nucleus is formed with priority is formed by selectively forming a region having a high concentration of silicon in an insulating film in contact with said amorphous semiconductor film.

[Claim 4] A method of manufacturing a semiconductor device as claimed in claim 1, characterized in that said region where a crystal nucleus is formed with priority is formed by forming a region of an alloy or a compound of said amorphous semiconductor film and a metal.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Application]

The present invention relates to a method of forming a polycrystalline silicon film of a so-called thin film transistor using the polycrystalline silicon film as an active layer.

[0002]

[Prior Art]

A thin film transistor using as an active element a semiconductor thin film formed on an insulating film is extremely advantageous in attempting high integration of an integrated circuit. Conventionally, Japanese Patent Application Laid-open Nos. Sho 60-62159 and Sho 61-116874 disclose relevant technology of this kind. Both of them disclose a thin film transistor formed on an ordinary MOS transistor. As disclosed in them, as a semiconductor thin film for forming a thin film transistor, a polycrystalline silicon film is often used due to its easiness in manufacturing.

[0003]

However, it has been found that characteristics of the polycrystalline silicon thin film transistor are considerably inferior to those of a device on single crystalline silicon, since crystal defects exist in grains and at grain boundaries of the polycrystalline silicon of the polycrystalline silicon thin film transistor. Therefore, steps to deal with this are taken including: (1) hydrotreatment where these crystal defects are electrically inactivated by hydrogen atoms; and (2) a method where polycrystalline silicon having a larger grain size is used to make smaller the

influence of the crystal grain boundaries on the electric characteristics.

[0004]

Recently, a method where amorphous silicon is crystallized in the solid phase has been developed. It has been found that the grain size, which is usually about 0.1 μm, becomes as large as 1 - 5 μm. A method of manufacturing a polycrystalline silicon thin film transistor utilizing this method is described in the following with reference to Fig. 2.

[0005]

First, as illustrated in Fig. 2(a), a silicon substrate 1 is prepared and an insulating film 2 and a gate electrode 3 are formed. Further, a gate insulating film 4 is formed thereon. The gate insulating film 4 may be, for example, a silicon oxide film formed by CVD, or may be formed by thermal oxidation of polycrystalline silicon used as the gate electrode. The film thickness is typically about 40 nm.

[0006]

An amorphous silicon film 5 with a thickness of 10 - 100 nm is formed thereon as illustrated in Fig. 2(b). The amorphous silicon film 5 may be formed by any of electron beam deposition, CVD, and silicon ion implantation into a polycrystalline silicon film.

[0007]

Then, as illustrated in Fig. 2(c), by carrying out heat treatment in N_2 at 550°C - 650°C for five to fifteen hours, solid phase crystallization is carried out to obtain a polycrystalline silicon film 5a having a crystal grain size of 1 - 5 μm.

[0008]

After that, as illustrated in Fig. 2(d), the polycrystalline silicon film 5a is patterned. Then, phosphorus ions are selectively implanted to form source/drain diffusion regions 7. Further, an interlayer insulating film 8 and a wiring electrode 9 are formed.

[0009]

[Problem to be solved by the Invention]

However, the method described in the above has a drawback in that the variation (deviation) in the transistor characteristics is large.

[0010]

According to this method, while a crystal grain of several μm can be obtained at a maximum, the size of a transistor using the crystal is about 1 μm. In this case, the transistor characteristics differ greatly depending on whether a grain boundary is included in a channel or not.

[0011]

Positions of crystal nuclei are not controlled, and thus, the grain size has a certain distribution. Therefore, whether a grain boundary is included in a channel or not is a random event

and totally uncontrollable.

[0012]

In order to eliminate the above-described problem of the variation in the characteristics accompanying an enlarged grain size, the present invention provides a method for controlling a crystal grain boundary such that the crystal grain boundary is aligned with a channel region of a transistor, thereby forming a transistor having excellent characteristics with a small variation.

[0013]

[Means for Solving the Problem]

In order to attain the aforementioned object, according to the present invention, in a method of manufacturing a polycrystalline thin film by solid phase growth, a position of a crystal nucleus is controlled by selectively forming a prioritized nuclear generation region and forming a crystal nucleus in the region with priority, and a region to be a channel region of a transistor is crystallized by solid phase growth from the prioritized nuclear generation region.

[0014]

[Action]

As described in the above, according to the present invention, since a prioritized nuclear generation region is selectively formed when solid phase crystallization is carried out, places where crystal nuclei are generated with priority can be formed with good

controllability, and thus, a crystal grain boundary existing in a channel region of a thin film transistor can be controlled.

[0015]

This makes it possible to suppress, to a minimum, the conventionally observed variation in the characteristics accompanying an enlarged grain size.

[0016]

[Embodiment]

A first embodiment according to the present invention is described in detail in the following using Fig. 1.

[0017]

First, similarly to the case of the prior art, a silicon substrate 1 having an insulating film 2, a gate electrode 3, and a gate insulating film 4 is prepared (Fig. 1(a)).

Then, an amorphous silicon film 5 with a thickness of 50 nm is formed. Next, a pattern for defining source/drain diffusion regions is formed using photoresist. Then, phosphorous ions are implanted under conditions of 1×10^{14} ions/cm^2 and 40keV to form heavily doped regions 6 (the regions are to be source/drain regions) (Fig. 1(b)).

After that, heat treatment is carried out in N_2 at 600°C for fifteen hours. Here, as illustrated in the relationship between time period of the heat treatment and crystalline fraction of Fig. 3, the more heavily doped the region is, the faster a crystal nucleus

is generated and the faster the crystallization is. Therefore, polycrystallization begins from the heavily doped regions 6. In other words, the heavily doped regions 6 are regions referred to as prioritized nuclear generation regions. Before crystallization begins in a lightly doped region (or an undoped region), crystallization of the heavily doped regions 6 is completed. Therefore, generation and growth of a nucleus in the lightly doped region are not carried out freely (randomly). Rather, the crystallization progresses by solid phase (epitaxial) growth with polycrystalline silicon 5a in the heavily doped regions 6 being as seeds. Thus, free (random) nuclear generation is not caused in a channel region sandwiched between the heavily doped regions 6, and the crystallization begins from the heavily doped regions 6 on both sides. This controls the position of a crystal grain boundary in the channel region and allows existence of only one crystal grain boundary at any time. (Fig. 1(c))

After that, the polycrystalline silicon film 5a is patterned /separated. Then, if necessary, heat treatment of the ion implantation seeds is carried out for activation. Further, an interlayer insulating film 8 and a wiring electrode 9 are formed. Further, if necessary, an additional interlayer insulating film and an additional wiring electrode may be formed to form multilayer wiring.

[0018]

Next, a second embodiment according to the present invention is described in detail using Fig. 5.

[0019]

First, similarly to the conventional case, a silicon substrate 1 having an insulating film 2, a gate electrode 3, and a gate insulating film 4 is prepared (Fig. 5(a)).

Then, silicon/ion implantation with the dose being about 10^{20} cm^{-2} is selectively carried out by ion implantation to form a region 10 having a high concentration of silicon from the surface of the insulating film 2 to both side portions of the gate insulating film 4. (Fig. 5(b))

Then, an amorphous silicon film 5 with a thickness of 50 nm is formed. (Fig. 5(c))

After that, heat treatment is carried out in N_2 at about 600°C for about fifteen hours. Here, since a crystal nucleus is generated faster in the region 10 having a high concentration of silicon, polycrystallization begins from the region 10 having a high concentration of silicon. In other words, the region 10 having a high concentration of silicon is a prioritized nuclear generation region. The crystallization progresses by solid phase (epitaxial) growth with the region 10 being as a seed to form a polycrystalline silicon film 5a. This controls the position of a crystal grain boundary in a region to be a channel and allows existence of only one crystal grain boundary at any time. (Fig. 5(d))

After that, the polycrystalline silicon film 5a is patterned /separated. Then, ion implantation/heat treatment for activation for forming a source/a drain are carried out, and further, an interlayer insulating film 8 and a wiring electrode 9 are formed. If necessary, an additional interlayer insulating film and an additional wiring electrode may be further formed to form multilayer wiring. (Fig. 5(e))

Further, a third embodiment is described using Fig. 6.

[0020]

First, similarly to the conventional case, a silicon substrate 1 having an insulating film 2, a gate electrode 3, and a gate insulating film 4 is prepared, and further, an amorphous silicon film 5 with a thickness of 50 nm is formed. (Fig. 6(a))

After that, metal films 11 with a thickness of about 20 - 50 nm are selectively formed on the amorphous silicon film 5 so as to overlap both side portions of the gate electrode 3 by a small amount. The method of forming them may be selective etching using photolithography technology, ion assisted CVD utilizing an ion beam, or the like. (Fig. 6(b))

After that, heat treatment is carried out in N_2 at about 600°C for about fifteen hours. Here, by appropriately selecting the kind of the metal films 11, the metal films 11 react with the amorphous silicon film 5 to form an alloy or an intermetallic compound. An example of the former is Au (gold), while examples of the latter

are Pt (platinum) and Pd (palladium). Since these metals become crystalline or polycrystalline when they react with amorphous silicon, crystallization progresses by solid phase (epitaxial) growth with the (poly)crystalline region, that is, a prioritized nuclear generation region, being as a seed to form a polycrystalline silicon film 5a. This controls the position of a crystal grain boundary in a region to be a channel and allows existence of only one crystal grain boundary at any time. (Fig. 6(c))

After that, the polycrystalline silicon film 5a is patterned /separated. Then, ion implantation/heat treatment for activation for forming a source/a drain are carried out, and further, an interlayer insulating film 8 and a wiring electrode 9 are formed. If necessary, an additional interlayer insulating film and an additional wiring electrode may be further formed to form multilayer wiring. (Fig. 6(d))

[0021]

In the embodiments described in the above, the prioritized nuclear generation regions are the same as the source/drain regions 7. However, the positional relationship between the heavily doped regions 6 and the source/drain regions 7 is not limited thereto. For example, as illustrated in Fig. 4(a), as far as the prioritized nuclear generation regions exclude the channel region and fully include the source/drain regions, by patterning the polycrystalline silicon film, the channel region and the source/drain regions can

be formed.

[0022]

Or, as illustrated in Fig. 4(b), as far as the prioritized nuclear generation regions are included in the source/drain regions, a similar crystal grain boundary can be formed.

[0023]

Further, prioritized nuclear generation regions may be outside an element region. In this case, by a process of separating the element region, the prioritized nuclear generation regions no longer influences the element region. For example, as illustrated in Fig. 4(c), when the prioritized nuclear generation regions are beside the channel region, a crystal grain boundary is generated in parallel with the direction of current of the channel, which makes it possible to make smaller the influence of the crystal grain boundary on the electric characteristics.

[0024]

Further, the present embodiments are examples where a gate electrode is below a channel region, that is, a so-called reverse-structured transistor. However, even in a forward-direction transistor, if a gate electrode and source/drain regions are formed using a different pattern (non-self-aligning manner), implementation almost similar to the present embodiments can be made.

[0025]

Further, with regard to a method where source/drain regions are formed in a self-aligning manner with respect to a gate electrode (self-aligning manner), the present invention is applicable if steps before the gate electrode is formed are carried out at or below a temperature where amorphous silicon is crystallized (about 550°C).

[0026]

Further, though embodiments where a MOS field effect transistor is used are described, the present invention is not limited thereto if a polycrystalline silicon thin film is used and there is a region to be a prioritized nuclear generation region. For example, the present invention is applicable to a junction field effect transistor, a bipolar transistor, a resistor, or the like.

[0027]

[Effect of the Invention]

As described in the above, according to the present invention, since a prioritized nuclear generation region is selectively formed when solid phase crystallization is carried out, places where crystal nuclei are generated with priority can be formed with good controllability, and thus, a crystal grain boundary existing in a channel region of a thin film transistor can be controlled.

[0028]

This makes it possible to suppress to a minimum the conventionally observed variation in the characteristics accompanying an enlarged grain size.

[0029]

Further, in the first embodiment, since what is done is only to carry out before the solid phase crystallization the ion implantation for forming the source/drain, what is conventionally carried out after the polycrystalline silicon film is formed, the number of the steps is not increased, and thus, the characteristics can be improved with the conventional number of the steps remaining the same.

[Brief Description of the Drawings]

[Fig. 1] First embodiment according to the present invention

[Fig. 2] Prior art

[Fig. 3] Relationship between time period of heat treatment and crystalline fraction

[Fig. 4] Examples of arrangement in an element formed according to the present invention

[Fig. 5] Second embodiment according to the present invention

[Fig. 6] Third embodiment according to the present invention

[Description of Symbols]

1 silicon substrate

2 insulating film

3 gate electrode

4 gate insulating film

5 amorphous silicon film

5a polycrystalline silicon film

6 heavily doped region

10 region having a high concentration of silicon

11 metal film